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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/870,446	06/01/2001	Michael Catherwood	18153.0046	8454

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EXAMINER	
GERSTL, SHANE F	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/870,446	CATHERWOOD, MICHAEL	
	Examiner	Art Unit	
	Shane F Gerstl	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 July 2004 and 10 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-4 and 6-13 have been examined.

Papers Received

2. Receipt is acknowledged of information disclosure statement and amendment papers submitted, where the papers have been placed of record in the file.

3. The objections to the claims, drawings, title, declaration, and information disclosure statement have all been overcome and are herein withdrawn. However, a new objection to the new information disclosure statement follows.

Information Disclosure Statement

4. All US and foreign patents references on the information disclosure statement have been considered as have items T, U, and V on page two of the information disclosure statement. The Examiner has not considered the remaining non-patent literature because it is not readily available to him. The CD that Applicant has sent with copies of the references is currently stored in a central warehouse and due to a recent move to a new facility delivery service has not yet been established to the new facility. The Examiner has done his best to cooperate with the situation by accessing the readily available foreign patent documents and the non-patent literature noted above. In the future, please submit paper copies of each foreign patent and non-patent literature document so that they can be scanned into the electronic system as CD copies are not scanned and thus submission of only a CD is not entirely proper. In the current case, please submit paper copies of each non-considered NPL document and considered items T and U from page 2 of the information disclosure statement so that they can be

scanned. The Examiner has printed copies of the foreign references for scanning and thus paper copies of those need not be submitted.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4 and 6-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cotton (3,771,146) in view of Appelt (3,886,524).

7. In regard to claim 1,

a. Cotton discloses a method of preventing processing errors due to pointer registers having invalid data, comprising:

i. fetching from a one of the pointer registers an instruction having a pointer operand for execution; [Column 8, lines 17-18 show that instructions are fetched. Column 5, lines 17-22 show that performance of each process (instruction or set of instructions) uses a capability register for a required access to memory (and thus holds an operand since the value is necessary for operation). Lines 24-44 show that the registers hole data that is based on a pointer table and thus the capability registers hold pointer operands.]

ii. determining whether a trap flag corresponding to the one of the pointer registers is in a set or reset condition; [Column 5, lines 24-27 and 45-48 show that the pointer register includes an access field (trap flag) for holding access code that is used for trapping a process. Column 17, lines 34-42 show a case where a trap is caused when the access code (trap flag) is '00' or reset, and thus the fact that the flag is in a reset condition was determined.]

iii. and generating a trap control signal when the trap flag is in a reset condition. [Column 17, lines 34-42 show a case where a trap is caused when the access code (trap flag) is '00' or reset. Column 11, lines 32-36 shows that the setting of the trap indicator causes a trap signal to be passed (and thus generated) to a control unit and it is thus a trap control signal.]

b. Cotton does not disclose setting trap flags associated with pointer registers to a reset condition after one of a power up of the processor or a reset of the processor, wherein the set condition indicates the one of the pointer registers has valid data and the reset condition indicates the one of the pointer registers has invalid data.

c. Appelt has disclosed in column 9, lines 30-48 that a TLPRES- signal is set to a reset condition of "low" ('0') after recognizing a rest of the processor will occur. This then causes a power-up interrupt trap to be performed and is thus indicates a trap and is a trap flag. This section also shows that it is set low to

clear all information and set logic to the idle state. This means that when the signal is set to low, the device information is invalid and must be reset. When the condition goes to high, the system is stable and data is validly idle (and after being restored valid for operation) and ready to be restored with the interrupt trap, also as shown in this section.

d. Appelt shows in this same section that this trap flag prohibits activity from occurring on the reset since the results will be unknown and cannot be processed correctly with a reset of power to the processor. The power-up trap is a recovery-type trap that allows for resuming of processing when there is stable power. This ability to prohibit activity when the processor is unstable and thus avoid errors would have motivated one of ordinary skill in the art to modify the design of Cotton to set the trap flag to a reset condition on a processor reset as taught by Appelt.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Cotton to incorporate the method of setting the trap flag to a reset condition on a processor reset as taught by Apelt so that data instability and processing errors are avoided.

8. In regard to claim 2, Cotton discloses the method according to claim 1, further comprising: triggering a trap interrupt based on the trap control signal. [Column 11, lines 29-36 show that the trap signal sent to the control unit triggers a trap micro-sequence to be performed. The heading given in column 10, line 16 shows that the trap operation is that of a trap interrupt.]

9. In regard to claim 3, Cotton discloses the method according to claim 1, further comprising: executing the instruction when the trap flag is in the set condition. [Column 2, lines 63-65 show that the processes (instructions) are executed. Further, column 4, lines 14-16 show an instruction that is executed. There are similar statements throughout the disclosure that indicate that the fetched instructions are in fact executed. As shown in the previous section of Appelt, this must take place when the flag is in the set condition indicating that power is up and stable and that the logic is valid for operation.]

10. In regard to claim 4, Cotton discloses the method according to claim 1, further comprising: changing the trap flag corresponding to the pointer from the reset condition to the set condition based upon a write of valid data to the pointer. [As shown in the sections cited above for claim 1, the access code (trap flag) indicates the access rights to the pointer section of the capability register. This is further shown in column 1, lines 13-26, which illustrates that the access code is for a certain pertinent capability word (pointer). This means that when the pointer changes, the access code (trap flag) corresponding to the pointer must inherently change as well so that it gives updated access rights to the memory section pointed to.]

11. In regard to claim 6,

a. Cotton discloses a method of preventing processing errors due to pointers having invalid data, comprising:

i. providing trap flags, each corresponding to a pointer register; [Column 5, lines 17-22 show that performance of each process uses a

capability register for a required access to memory. Lines 24-44 show that the registers hole data that is based on a pointer table and thus the capability registers hold pointer operands. Column 5, lines 24-27 and 45-48 show that the pointer register includes an access field (trap flags) for holding access code that is used for trapping a process.]

ii. setting the trap flags to a reset condition; [Column 5, lines 53-58 show that the capability is register (which includes the trap flags or access code) is reset on various conditions.]

iii. and setting the trap flag corresponding to each pointer register based on valid data being written to the pointer register. [As shown in the sections cited above, the access code (trap flag) indicates the access rights to the pointer section of the capability register. This is further shown in column 1, lines 13-26, which illustrates that the access code is for a certain pertinent capability word (pointer). This means that when the pointer changes, the access code (trap flag) corresponding to the pointer must inherently change as well so that it gives updated access rights to the memory section pointed to.]

b. Cotton does not disclose that the resetting of the trap flags is based on a power-up or reset.

c. Appelt has disclosed in column 9, lines 30-48 that a TLPRES- signal is set to a reset condition of "low" ('0') after recognizing a rest of the processor will

occur. This then causes a power-up interrupt trap to be performed and is thus indicates a trap and is a trap flag.

d. Appelt shows in this same section that this trap flag prohibits activity from occurring on the reset since the results will be unknown and cannot be processed correctly with a reset of power to the processor. The power-up trap is a recovery-type trap that allows for resuming of processing when there is stable power. This ability to prohibit activity when the processor is unstable and thus avoid errors would have motivated one of ordinary skill in the art to modify the design of Cotton to set the trap flag to a reset condition on a processor reset as taught by Appelt.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Cotton to incorporate the method of setting the trap flag to a reset condition on a processor reset as taught by Apelt so that data instability and processing errors are avoided.

12. In regard to claim 7, Cotton in view of Appelt discloses the method according to claim 6, further comprising: generating a trap control signal when an instruction causes the processor to read a pointer register having a corresponding trap flag set to the reset condition. [Column 17, lines 34-42 show a case where a trap is caused when the access code (trap flag) is '00' or reset. Column 11, lines 32-36 shows that the setting of the trap indicator causes a trap signal to be passed (and thus generated) to a control unit and it is thus a trap control signal.]

13. In regard to claim 8, Cotton in view of Appelt discloses the method according to claim 7, further comprising: triggering a trap interrupt based on the trap control signal. [Column 11, lines 29-36 show that the trap signal sent to the control unit triggers a trap micro-sequence to be performed. The heading given in column 10, line 16 shows that the trap operation is that of a trap interrupt. Further, Appelt shows in column 9, lines 46-48 that the power-up trap is an interrupt trap.]

14. In regard to claim 9,

a. Cotton discloses a processor having logic that prevents processing errors due pointer registers having invalid data, comprising:

i. instruction fetch and decode logic for fetching and decoding instructions; [Column 8, lines 17-18 show that instructions are fetched and thus there is instruction fetch logic. The decoding logic is inherent since the processor executes instructions or processes, as discussed in both the background and general description sections, and there must be decoding logic to interpret the machine instructions in order to recognize the operation to be performed and the operands to use for the operation.]

i. registers for holding data; [Column 5, lines 17-22 show that performance of each process (instruction or set of instructions) uses a capability register (which inherently holds data) for a required access to memory.]

ii. trap flags associated with the registers, each trap flag corresponding to a one of the registers and each trap flag indicating a set

or reset condition; [Column 5, lines 24-27 and 45-48 show that the pointer register includes an access field (trap flag) for holding access code that is used for trapping a process. Column 17, lines 34-42 show a case where a trap is caused when the access code (trap flag) is '00' or reset. Column 10, lines 5-15 show that the access code (trap flags) are manipulated to determine if they are in a set or reset condition (a '1' or '0').]

ii. and a pointer trap coupled to the trap flags, the pointer trap generating a trap control signal based on decoding an instruction that reads a one of the registers that has a corresponding trap flag in the reset condition. [Lines 24-44 show that the registers hole data that is based on a pointer table and thus the capability registers hold pointer operands. Column 17, lines 34-42 show a case where a trap is caused when the access code (trap flag) is '00' or reset. Column 11, lines 32-36 shows that the setting of the trap indicator causes a trap signal to be passed (and thus generated) to a control unit and it is thus a trap control signal.]

b. Cotton does not disclose wherein the trap flags are in a reset condition after a power up or reset and in the set condition after valid data is written to the associated register, whereby the trap flag in the rest condition indicates the register has invalid data.

c. Appelt has disclosed in column 9, lines 30-48 that a TLPRES- signal is set to a reset condition of "low" ('0') after recognizing a rest of the processor will occur. This then causes a power-up interrupt trap to be performed and is thus

indicates a trap and is a trap flag. This section also shows that it is set low to clear all information and set logic to the idle state. This means that when the signal is set to low, the device information is invalid and must be reset. When the condition goes to high, the system is stable and data is validly idle (and after being restored valid for operation) and ready to be restored with the interrupt trap, also as shown in this section.

d. Appelt shows in this same section that this trap flag prohibits activity from occurring on the reset since the results will be unknown and cannot be processed correctly with a reset of power to the processor. The power-up trap is a recovery-type trap that allows for resuming of processing when there is stable power. This ability to prohibit activity when the processor is unstable and thus avoid errors would have motivated one of ordinary skill in the art to modify the design of Cotton to set the trap flag to a reset condition on a processor reset as taught by Appelt.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Cotton to incorporate the method of setting the trap flag to a reset condition on a processor reset as taught by Apelt so that data instability and processing errors are avoided.

15. In regard to claim 10, Cotton discloses the processor according to claim 9, wherein the trap control signal is only generated when the register being read from is being used as a pointer register. [As shown above, the registers being read from are pointer registers.]

16. In regard to claim 11, Cotton discloses the processor according to claim 9, further comprising interrupt logic for generating an interrupt based on the trap control signal. [Column 11, lines 29-36 show that the trap signal sent to the control unit triggers a trap micro-sequence to be performed. The heading given in column 10, line 16 shows that the trap operation is that of a trap interrupt.]

17. In regard to claim 12,

a. Cotton discloses the processor according to claim 9, further comprising: resetting the trap flags. [Column 5, lines 53-58 show that the capability is register (which includes the trap flags or access code) is reset on various conditions.]

b. Cotton does not disclose a reset/power up unit coupled to the trap flags, wherein the reset/power on unit causes the trap flags to be in the reset condition upon a reset/power up.

c. Appelt has disclosed in column 9, lines 30-48 that a TLPRES- signal is set to a reset condition of "low" ('0') after recognizing a rest of the processor will occur. This then causes a power-up interrupt trap to be performed and is thus indicates a trap and is a trap flag. There inherently exists reset logic or a rest unit in this disclosure to perform this resetting of the trap flags.

d. Appelt shows in this same section that this trap flag prohibits activity from occurring on the reset since the results will be unknown and cannot be processed correctly with a reset of power to the processor. The power-up trap is

a recovery-type trap that allows for resuming of processing when there is stable power. This ability to prohibit activity when the processor is unstable and thus avoid errors would have motivated one of ordinary skill in the art to modify the design of Cotton to set the trap flag to a reset condition on a processor reset using a reset unit as taught by Appelt.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Cotton to incorporate the method of setting the trap flag to a reset condition on a processor reset using a reset unit as taught by Apelt so that data instability and processing errors are avoided.

18. In regard to claim 13,

a. Cotton discloses the processor according to claim 9, further comprising: a trap flag control unit coupled to the trap flags, wherein the trap flag control unit causes the trap flags to be in the reset condition and to be in the set condition when the corresponding registers have valid data written thereto. [Column 5, lines 53-58 show that the capability is register (which includes the trap flags or access code) is reset on various conditions. As shown in the sections cited above for claim 1, the access code (trap flag) indicates the access rights to the pointer section of the capability register. This is further shown in column 1, lines 13-26, which illustrates that the access code is for a certain pertinent capability word (pointer). This means that when the pointer changes, the access code (trap flag) corresponding to the pointer must inherently change as well so that it gives

updated access rights to the memory section pointed to. This is all inherently accomplished using logic for setting the trap flags or a trap flag control unit.]

b. Cotton does not disclose resetting the trap flags upon a reset/power up.

c. Appelt has disclosed in column 9, lines 30-48 that a TLPRES- signal is set to a reset condition of "low" ('0') after recognizing a rest of the processor will occur. This then causes a power-up interrupt trap to be performed and is thus indicates a trap and is a trap flag. There inherently exists reset logic or a rest unit in this disclosure to perform this resetting of the trap flags.

d. Appelt shows in this same section that this trap flag prohibits activity from occurring on the reset since the results will be unknown and cannot be processed correctly with a reset of power to the processor. The power-up trap is a recovery-type trap that allows for resuming of processing when there is stable power. This ability to prohibit activity when the processor is unstable and thus avoid errors would have motivated one of ordinary skill in the art to modify the design of Cotton to set the trap flag to a reset condition on a processor reset using a reset unit as taught by Appelt.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Cotton to incorporate the method of setting the trap flag to a reset condition on a processor reset using a reset unit as taught by Apelt so that data instability and processing errors are avoided.

Response to Arguments

19. Applicant's arguments filed 7/19/04 have been fully considered but they are not persuasive.

20. Applicant has argued throughout the remarks that the disclosed references are faulty because they do not disclose the registers being volatile memory, however, this is not claimed and the claim limitations, not the disclosure, are the measure of the invention and thus the argument is moot.

21. Applicant has also argued that the references do not teach preventing program operation if an address pointer register may not have valid address data therein. Again, the claims do not define that program operation is prevented.

22. Applicant has also argued that Cotton does not suggest causing all traps flags associated with volatile registers to be reset and that only flags associated with point registers are set. Again, the claims do not specify these limitations.

23. Applicant has argued that Appelt does not teach or suggest causing a specific trap flag to be in a set condition when its associated pointer register is written to with valid data program address information. On the contrary, the section of column 9 shows that when the flag is in the set condition, system conditions are stable and a power-up interrupt trap is performed to restore state and thus write valid data to the registers.

24. Applicant then argues that Appelt does not teach or suggest checking a trap flag before using the data contained in an associated pointer register for program address information. Again, this limitation is not claimed. It is only claimed that data is used when the flag is in a set condition. There is no mention of checking the flag at a specific

moment before data can be used, but simply that there is a time when the condition is set and data is used.

Conclusion

25. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

26. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The references cited previously remain pertinent and are cited herein as well.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-4166. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shane F Gerstl
Examiner
Art Unit 2183

SFG
October 15, 2004

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